

A cross-sectional view of a semiconductor device. The device is divided into three regions: SOLID-STATE IMAGE PICKUP REGION, PERIPHERAL CIRCUIT REGION TRANSISTOR PORTION, and PERIPHERAL CIRCUIT REGION P WELL CONTACT PORTION. The device consists of a substrate 601, a gate layer 602, and a conductive layer 615. The gate layer 602 is shown as a series of rectangular blocks, and the conductive layer 615 is shown as a series of rectangular blocks on top of the gate layer 602.

FIG. 2B  
(PRIOR ART)

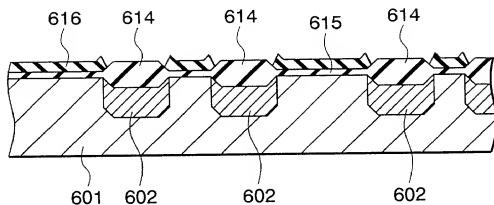


FIG. 2C  
(PRIOR ART)

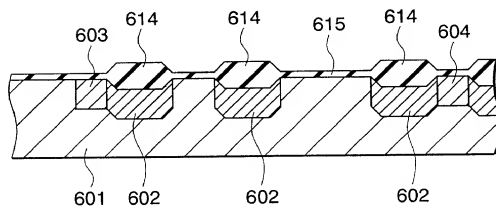


FIG. 2D  
 (PRIOR ART)

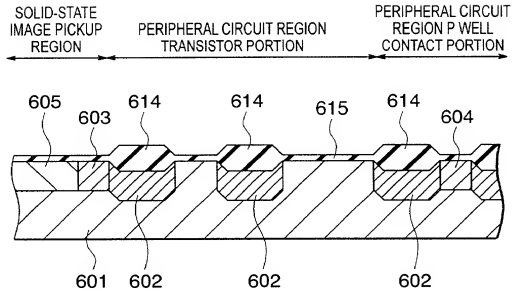


FIG. 2E  
 (PRIOR ART)

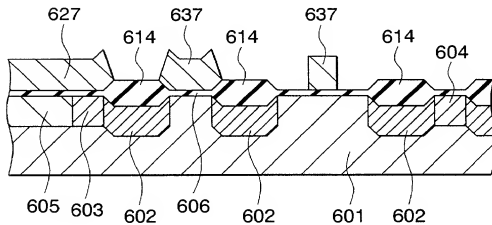


FIG. 2F  
 (PRIOR ART)

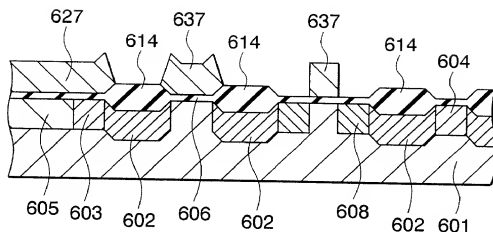


FIG. 2G  
 (PRIOR ART)

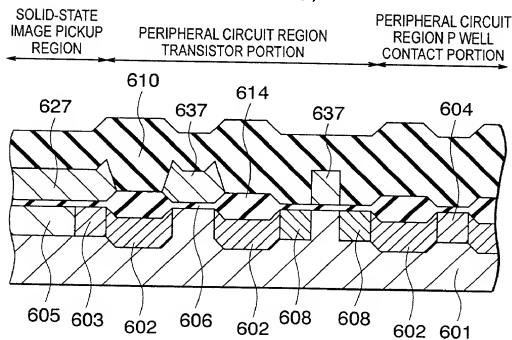


FIG. 2H  
 (PRIOR ART)

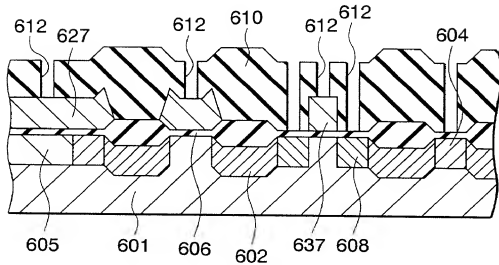


FIG. 3

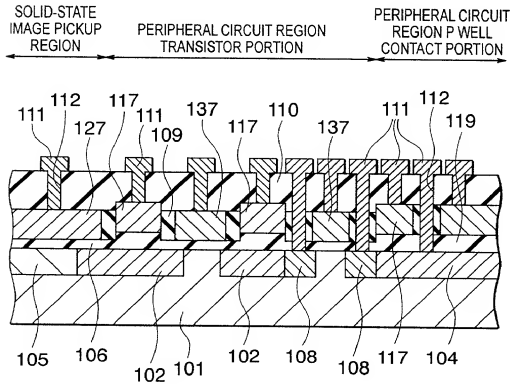


FIG. 4A

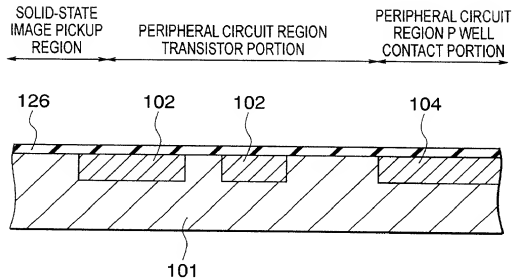


FIG. 4B

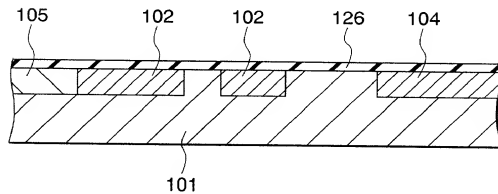


FIG. 4C

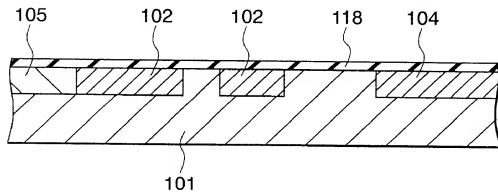


FIG. 4D

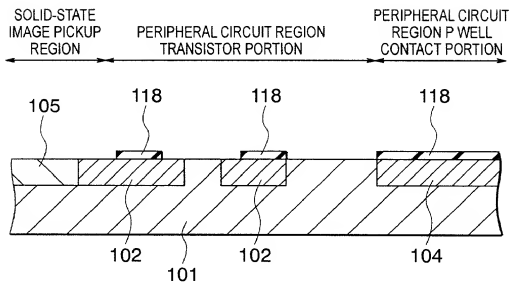


FIG. 4E

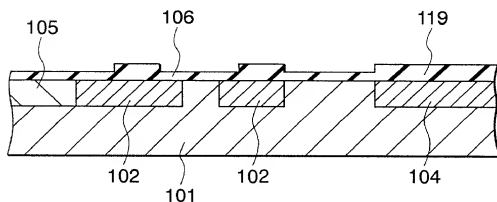
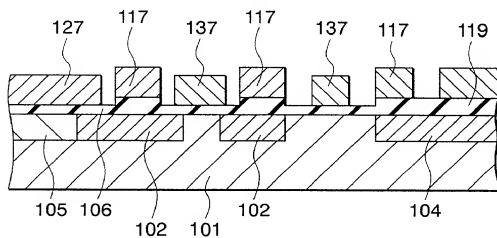


FIG. 4F



This cross-sectional view illustrates the device structure. The **SOLID-STATE IMAGE PICKUP REGION** on the left contains a stack of layers 105 and 106, with a channel layer 102 and a substrate 101. The **PERIPHERAL CIRCUIT REGION TRANSISTOR PORTION** in the center features a channel layer 102 and a substrate 101, with gate structures 117 and 137. The **PERIPHERAL CIRCUIT REGION P WELL CONTACT PORTION** on the right includes a p-well layer 104 and a substrate 108, with contact structures 117 and 119. A dashed line indicates a boundary or interface between the transistor and p-well regions.

[illegible]

This cross-sectional view shows a multi-layered semiconductor structure. The top layer is labeled 127. Below it is a layer with alternating blocks labeled 109 and 117. A layer labeled 137 is positioned below the 109/117 blocks. Another layer with alternating blocks labeled 117 and 137 is shown below that. The bottom-most layer is labeled 119. The entire structure is supported by a substrate with layers labeled 105, 106, 102, 101, 102, 108, 108, and 104 from top to bottom.



FIG. 4J

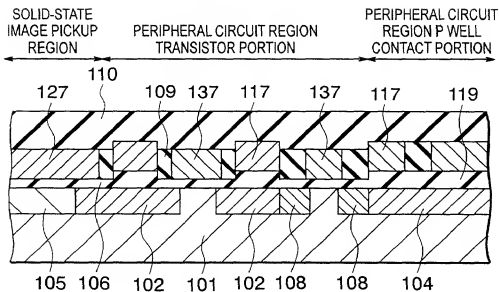


FIG. 4K

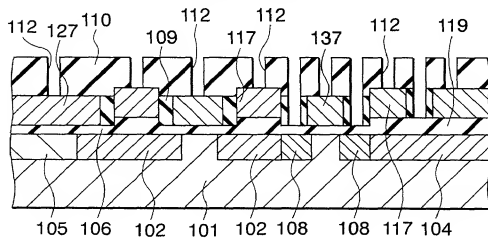


FIG. 4L

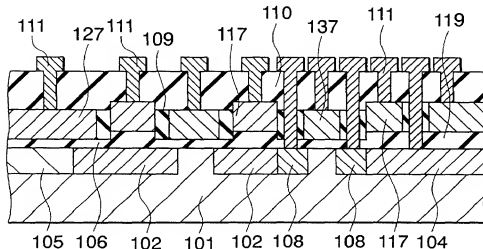


FIG. 5

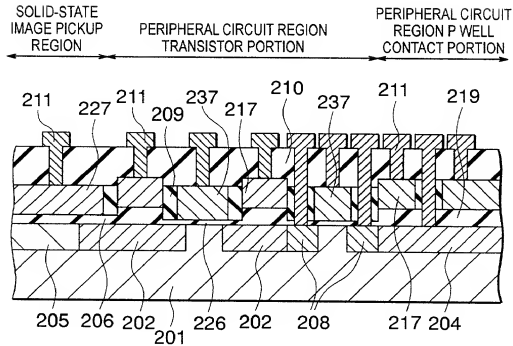


FIG. 6

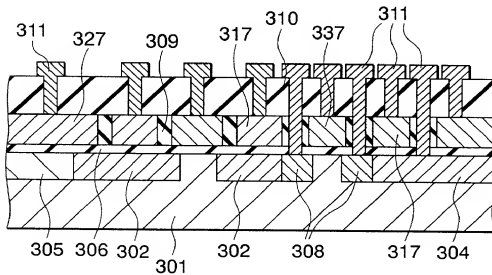


FIG. 7

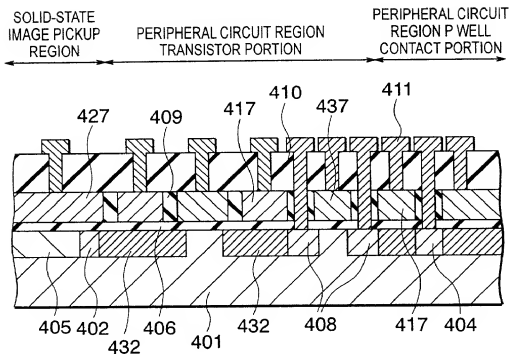


FIG. 8

